SHM-PWAM Control Strategy Applied to a Five-Level Flying-Capacitor Inverter

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Abstract

Compared to the conventional selective harmonic mitigation-pulse width modulation (SHM-PWM), the selective harmonic mitigation-pulse width and amplitude modulation (SHM-PWAM) control strategy for multilevel inverters has considerable advantages such as improved output harmonics contents and reduced power dissipation. These are due to the optimization of dc sources values along with the optimized angles. However, realizing the SHM-PWAM needs the regulation of dc sources in different values with acceptable dynamic response. The flying capacitor multilevel inverter (FCMLI) has the ability of the dc voltages self-balancing due to its switching state redundancies so a promising topology for the realization of the SHM-PWAM. In this paper, the SHM-PWAM control strategy is applied to a five-level FC-MLI. Simulation results show the priority of PWAM over the conventional PWM from the total harmonic distortion (THD) improvement and power dissipation reduction points of view.

Keywords: FCMLI, PAM, PWAM, PWM, THD, Voltage balancing.

1. Introduction

Multilevel converters have attracted the attention of many researchers and industry in medium voltage and high power applications in recent years. This is due to their various benefits compared to two-level inverters such as reducing the voltage stress on
semiconductor switches, reducing the total harmonic distortion (THD), reducing the common mode voltage and requiring a smaller output filter [1, 2]. Three basic structures of multilevel inverters are: diode-clamped, flying capacitor and cascaded H-bridge (CHB) [2]. Generally, multilevel inverter control methods are classified in two categories: high frequency and low frequency. In applications where the switching losses are not of importance, high frequency Control methods such as carrier-based pulse-width modulation (CB-PWM) is very effective. Harmonics generated by these methods are set far from the system fundamental frequency and so it is easier to filter them.

However, in high power ratings, the power dissipation during the switching and conduction modes limits the switching frequency. Under this condition, the low frequency control techniques such as selective harmonic elimination pulse-width modulation (SHE-PWM) and selective harmonic mitigation pulse width modulation (SHM-PWM) should be used [3,4]. The main purpose of these control methods is to generate a switching pulse pattern in such a way that a desired output fundamental is produced while specific selective harmonic levels are eliminated or mitigated [5]. However, setting the low order harmonics equal to zero in the SHE-PWM strategy may leave the first non-eliminated harmonics contents uncontrolled. This is a great disadvantage which makes the results unsuitable for use in actual applications due to the need for large output filter which increases the cost and size of the system [5].

In order to overcome the mentioned disadvantage, SHM techniques were introduced in which instead of setting the harmonics contents to zero, their limits are met by the grid codes (i.e. CIGRE WG 36-05 [6] and EN 50160 [7]). In this way the generated output waveform fully meets the grid codes requirements using smaller output filters or even lower switching frequencies compared to the SHE [4, 8]. Recently, a modulation method has been proposed in [5] which applies the combination of pulse-width and pulse-amplitude modulations. In other words, the pulse amplitude modulation (PAM), which is mainly used
in telecommunications systems, is applied simultaneously with PWM to the CHB inverter. It means that the CHB dc sources values have also been optimized along with the switching angles. In this way the system degrees of freedom increase without increasing the switching frequency and its related power loss. Applying this proposed control strategy resulted in significant improvements in the system performance such as THD and power loss. However, realizing the SHM-PWAM needs the regulation of dc sources in different optimized values with acceptable dynamics. This necessity has been met in [9] by means of a PWM rectifier inverter system. The FCMLI has the ability of the dc voltages self-balancing due to its switching state redundancies so a promising topology for the realization of the SHM-PWAM without any additional or auxiliary circuits.

In this paper, the SHM-PWAM control strategy is applied to a five-level FC-MLI. Here, the number of freedom degrees is considered seven which six of them are the switching angles and one is the dc source value. Simulation results show the ability of this method in satisfying the grid codes requirements. Also the priority of this method has been proved from the THD improvement and power loss reduction points of view compared to the conventional SHM-PWM. Section II introduces the FCMLI and control methods for flying capacitor voltage. The third section introduces the SHM-PWM and SHM-PWAM control principles. Simulation results are then carried out in Section IV.

2. Flying Capacitor Multilevel Inverter

2.1. Basic configuration

The FC-MLI requires a large number of capacitors to clamp the device (switch) voltage to one capacitor voltage level. Provided all the capacitors are of equal value, an $n$-level inverter will require a total of $(n-1) \times (n-2)/2$ clamping capacitors per phase leg in addition to $(n-1)$ main dc bus capacitors. The size of the voltage increment between two consecutive legs of the clamping capacitors defines the size of voltage steps in the output.
waveform. Let us consider the group of capacitors in a single clamping leg as one equivalent capacitor, then for an \( n \)-level inverter, if the voltage of the main dc-link capacitor is \( V_{dc} \), the voltage of the innermost capacitor clamping the innermost two devices is \( V_{dc}/(n-1) \). The voltage of the next innermost capacitor will be \( V_{dc}/(n-1)+V_{dc}/(n-1)=2V_{dc}/(n-1) \) and so on. Each next clamping capacitor will have the voltage increment of \( V_{dc}/(n-1) \) from its immediate inner one. The voltage levels and the arrangements of the flying capacitors in the FCMLI structure assures that the voltage stress across each main device is same and is equal to \( V_{dc}/(n-1) \), for an \( n \)-level inverter.

Fig. 1 shows one phase leg of a five-level inverter. For a 3-phase inverter, two more legs of same construction are coupled to the same dc link battery \( V_{dc} \). In this figure each switch \( S_1 \) to \( S_4 \) and \( S_{11} \) to \( S_{41} \) consists of a power semiconductor device (e.g. GTO, IGBT) and an anti-parallel diode. Voltages \( V_{C4} \), \( V_{C3} \), \( V_{C2} \) and \( V_{C1} \) are \( 4V_{dc}/4 \), \( V_{dc}/2 \), \( 3V_{dc}/4 \) and \( V_{dc} \) respectively, as \( n=5 \) [1,10].

Figure 1: One phase leg of a five-level FCMLI.

The switch combinations given in Table 1 are used to synthesize the output voltage of phase-a, \( V_{an} \), with respect to the neutral point \( n \). The main dc capacitor combination, \( C_1 \) is
the energy storage element, while capacitors $C_2$, $C_3$ and $C_4$ are the flying capacitors that provide the multilevel voltage ability to the converter. The pairs of the switches $(S_1, S_{11})$, $(S_2, S_{21})$, $(S_3, S_{31})$ and $(S_4, S_{41})$ are closed in complementary manner. Thus if $S_1$ is ON, $S_{11}$ is OFF and vice-versa.

Table 1: Switching scheme for one phase leg of a five-level FCMLI.

<table>
<thead>
<tr>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$S_3$</th>
<th>$S_4$</th>
<th>$C_2$</th>
<th>$C_3$</th>
<th>$C_4$</th>
<th>$V_{dc}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>$V_{dc}/2$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>NC</td>
<td>NC</td>
<td>+</td>
<td>$V_{dc}/4$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>NC</td>
<td>+</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>+</td>
<td>-</td>
<td>NC</td>
<td>$V_{dc}/4$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>NC</td>
<td>-</td>
<td>NC</td>
<td>-</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>+</td>
<td>-</td>
<td>$-V_{dc}/4$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>-</td>
<td>NC</td>
<td>+</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>+</td>
<td>-</td>
<td>NC</td>
<td>$-V_{dc}/4$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>NC</td>
<td>+</td>
<td>NC</td>
<td>-</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>+</td>
<td>NC</td>
<td>NC</td>
<td>$-V_{dc}/2$</td>
</tr>
</tbody>
</table>

NC indicates that there is no change in the state of the corresponding capacitor, i.e., the capacitor neither charges nor discharges in this mode. The states + and − respectively denote the charging and discharging of the corresponding capacitors. The switching states given are for the positive half cycle of the outgoing current waveform (indicated as $i_a$ in
Fig. 1). The capacitor states (+ & -) will reverse for the negative half cycle of the current. We see from table 1 that the structure offers multiple switching combinations for $V_{an}$ equal to $V_{dc}/4$, $0$, and $-V_{dc}/4$ [11, 12].

2.2. **Flying capacitor voltage control:** To balance and regulate the capacitor voltages at their desired values, the following methods have been proposed in the technical literature:

- The first method is based on open-loop control methods [10], [13-18] and can be applied only to high frequency PWM techniques. The open-loop control methods are mostly based on the phase-shifted (PS)-PWM method, which has an inherent natural self-balancing property. However, in practice, due to non-idealities, system imbalance, and disturbance, an external control loop and an additional compensation algorithm are required to balance the capacitor voltages.

- The second method is based on using extra power circuitry in combination with the open-loop control methods (e.g., using RLC filters) to improve the voltage stabilization of the open-loop voltage balancing strategies [16]-[20]. This approach adds to the system cost, complexity, and lowers the efficiency.

- The third method is based on the closed-loop methods which modify the converter switching patterns to implicitly balance and maintain the capacitor voltages at their desired reference values [21]–[30]. It can be applied to both high and low frequency control strategies and is realized in two ways: 1- All the capacitors' voltages should be sensed and compared with their reference values. 2- Some of the capacitors' voltages are sensed and others are estimated or predicted.
3. The SHM-PWM and SHM-PWAM principles

The low-frequency output voltage of a five-level inverter is shown in Fig. 2. This is the programmed waveform with six switching angles \( \alpha_1, \ldots, \alpha_6 \) and one variable dc source voltage \( V_1 \).

The Fourier series of Fig. 2 can be written as:

\[
v(t) = \frac{1}{2}a_0 + \sum_{n=1}^{\infty} \left( a_n \cos n\omega_0 t + b_n \sin n\omega_0 t \right)
\]

where \( \omega_0 = \frac{2\pi}{T} \) and coefficients \( a_n \) and \( b_n \) can be calculated according to the following equations:

\[
a_n = \frac{1}{\pi} \int_{-\pi}^{\pi} f(\theta) \cos(n\theta) d\theta
\]

\[
b_n = \frac{1}{\pi} \int_{-\pi}^{\pi} f(\theta) \sin(n\theta) d\theta
\]

Due to the half-wave symmetry of the waveform, all \( a_n \) and even-numbered \( b_n \) coefficients are zero. The \( n^{th} \) harmonic can be mitigated if its related \( b_n \) coefficient is set equal to its minimum value. In addition, for a three-phase system, the triple-\( n \) harmonics in
the phase voltage are canceled out in the line voltage. Therefore, the low order harmonics to be mitigated are odd, non-triple-\(n\) harmonics starting as 5, 7, 11, 13, 17 …

The odd coefficients of \(b_n\) are:

\[
b_n = \frac{4}{n\pi} \left( V_1 (\cos n\alpha_1 - \cos n\alpha_2 + \ldots - \cos n\alpha_6) + 2V_1 (\cos n\alpha_4 - \cos n\alpha_5 + \cos n\alpha_6) \right) \quad (4)
\]

It should be noted that in the conventional SHM-PWM method the value of \(V_1\) is equal to \(V_{dc}\), therefore the desired coefficients of \(b_n\) can be written as:

\[
b_n = \frac{4V_{dc}}{n\pi} (\cos n\alpha_1 - \cos n\alpha_2 + \ldots - \cos n\alpha_6) + 2(\cos n\alpha_4 - \cos n\alpha_5 + \cos n\alpha_6) \quad (5)
\]

The SHM-PWM technique is based on the idea that it is not necessary to reduce to zero the harmonics while they are kept below the acceptable levels. These levels are defined by the grid codes which establish the maximum allowed limits for each harmonic order and THD in order to maintain the quality of the grid. The SHM-PWM technique is based on solving the following inequality system, where \(L_j\) is the maximum allowed level imposed by the applied grid code [8]:

\[
E_j = |M_a - b| \leq L_j
\]

\[
E_j = \frac{4V_{dc}}{|b|} \left[ (\cos j\alpha_1 - \cos j\alpha_2 + \ldots - \cos j\alpha_6) + 2(\cos j\alpha_4 - \cos j\alpha_5 + \cos j\alpha_6) \right] \leq L_j
\]

\[
j = 5, 7, 11, \ldots, 49
\]

The relationship between the dc link voltage of the converter and the amplitude of the generated fundamental component is called the modulation index \((M_a)\) and can be defined as \(M_a = b/4V_{dc}\) [31].

The above inequality (6) can be merged with an objective function \((OF)\) which should be minimized by the optimization algorithms.

\[
OF = (\alpha_1, \ldots, \alpha_6) = \sum_{j=5, 7, 11, \ldots, 49} E_j^2 + THD
\]

The constraints used are as follows:
\[ \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \frac{\pi}{2} \]  
\[ \alpha_{i+1} - \alpha_i > \delta (i = 1,2...,5) \]  
\( \delta \) is the minimum allowable pulse width and is assumed to be 0.01 rad. In the SHM-PWAM control strategy, the dc sources values are also defined as degrees of freedom along with the switching angles. They can be varied between the zero and 1 p.u. values.

In this way the inequality presented in (6) is rewritten as:

\[ E_i = |M_i - b| \leq L_i \]

\[ E_j = \frac{1}{|b_j|} \left\{ \frac{4V_1}{j\pi} \left[ \cos j\alpha_1 - \cos j\alpha_2 + \ldots - \cos j\alpha_6 \right] + 2 \left[ \cos j\alpha_4 - \cos j\alpha_5 + \cos j\alpha_6 \right] \right\} \leq L_j \]

\[ j = 5,7,11,...,49 \]  
\[ OF = (\alpha_1,...,\alpha_6,V_i) = \sum_{i=1,5,7,...,49} E_i^2 + THD \]  

Constraints are the same as (8) and (9). However an extra constraint should be added due to the dc source variability:

\[ 0 \leq V_i \leq 1 \]  

4. Simulation results

In this section a three-phase five-level FCMLI (Fig. 3.) realizing both the SHM-PWAM (case 1) and SHM-PWM (case 2) control strategies is simulated. These two cases are compared from the THD, power loss and the optimization algorithm feasibility points of view. Table 2 shows the simulated system parameters.

Both cases objective functions (equations (7) and (11)) are optimized by genetic algorithm (GA). The optimized answers are then saved to a lookup table (LUT).
Figure 3: Five-level FCMLI realizing SHM-PWAM method.

Table 2: The simulated system parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output frequency</td>
<td>50Hz</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>300Hz</td>
</tr>
<tr>
<td>Inductive-resistive load</td>
<td>10Ω and 15mH</td>
</tr>
<tr>
<td>Maximum input voltage</td>
<td>100 V</td>
</tr>
<tr>
<td>Flying capacitor value</td>
<td>1mF</td>
</tr>
</tbody>
</table>
Fig. 4 shows the first component magnitude of the output voltage waveform versus $M_a$ in both cases. It can be seen that GA is feasible in the whole range of $M_a$ for the SHM-PWAM case whereas the feasibility region for the conventional case is limited to $M_a > 0.32$. This is due to the extra degree of freedom applied to the system.

Fig. 5 shows the optimized switching angles in both cases and also the optimized dc source voltage value in case 1. Again it should be noted that this value is equal to 1 p.u. in the conventional SHM-PWM case.
As can be seen from the Figure, the optimized value of $V_1$ is increasing linearly as $M_a$ increases. This makes the variable dc source capable of changing evenly and also with a good dynamic response.

In the computing process the limits specified in the EN 50160 and CIGRE WG 36-05 grid codes have been considered but any other could have been chosen. These standards include specific limits for each harmonic up to 49th harmonic. The output waveform THD is calculated up to 40th harmonic. Table 3 shows the harmonic limits specified in the mentioned standards [31].
The output line voltage THD in both cases is depicted in Fig. 6. Comparing the THD diagrams proves the priority of the SHM-PWAM strategy over the conventional SHM-PWM in THD improvement. Moreover, it demonstrates the considerable THD reduction under increasing an extra degree of freedom. The grid code requirement is now well satisfied for THD over the whole range of \( M_a \).

Table 3: Gridcodeen 50160 requirements + quality grid code CIGRE WG 36–05[32].

<table>
<thead>
<tr>
<th>Standard</th>
<th>EN 50160</th>
<th>CIGRE JWG C4.07</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage level</td>
<td>1-35 kV</td>
<td>1-35 kV</td>
</tr>
<tr>
<td>Order</td>
<td>( h \leq 25 )</td>
<td>( h \leq 25 )</td>
</tr>
<tr>
<td>5</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>7</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>11</td>
<td>3.5</td>
<td>3.5</td>
</tr>
<tr>
<td>13</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>17</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>19</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>23</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>25</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>( h &gt; 25 )</td>
<td>( 0.2 + 32.5/h )</td>
<td>( 0.2 + 32.5/h )</td>
</tr>
<tr>
<td>THD up to 40th</td>
<td>8%</td>
<td>8%</td>
</tr>
</tbody>
</table>

Table 4: Solutions of the optimized equations (7) and (11) under two different conditions for both cases.

<table>
<thead>
<tr>
<th>( M_a )</th>
<th>( \alpha_1 ) (rad)</th>
<th>( \alpha_2 ) (rad)</th>
<th>( \alpha_3 ) (rad)</th>
<th>( \alpha_4 ) (rad)</th>
<th>( \alpha_5 ) (rad)</th>
<th>( \alpha_6 ) (rad)</th>
<th>( V_i ) (p.u.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.32 (case 1)</td>
<td>0.126</td>
<td>0.172</td>
<td>0.203</td>
<td>0.368</td>
<td>0.401</td>
<td>0.447</td>
<td>0.265</td>
</tr>
<tr>
<td>0.32 (case 2)</td>
<td>1.019</td>
<td>1.055</td>
<td>1.097</td>
<td>1.26</td>
<td>1.268</td>
<td>1.569</td>
<td>1</td>
</tr>
</tbody>
</table>
Fig. 6: Line voltage THD versus $M_a$

Fig. 7 shows the comparison between two cases from the line worst THD and worst harmonics contents points of view. The maximum allowed amounts from grid code have also been shown in the figure for better evaluation.

It can be concluded from the bars that in the conventional SHM-PWM, the filtering elements needed in the tuned filters are more bulky, heavy, and expensive in low-order harmonics. In contrast, the extra degree of freedom in SHM-PWAM gives more flexibility to the system performance and lets the designer choose a lower size output filter.

Figs. 8 and 9 show the five-level FCMLI output and line voltage waveforms for $M_a = 0.32$ in both cases. Solutions of the optimized equations (7) and (11) have been listed in Table 4.

As can be seen from Fig. 9, although the conventional SHM-PWM technique is able of producing the first component ($0.32\, p.u.$) the output line voltage level is reduced to five instead of nine due to the narrow pulse deletion phenomena. This drawback does not take place in case 1 as the dc sources values are variable for different modulation indices.
In order to compare the switching loss in both cases under equal load conditions, the reduction percentage of the switching loss in case 1 is calculated. The conduction loss in both cases are the same since it depends on the values of the switch collector – emitter
The switching loss for each switch can be obtained from equation (13).

\[
P_{SW} = f_{SW} V_{dc} I_{SW(pk)} (t_{SW(on)} + t_{SW(off)})
\]

\[
P_{rr} = 0.125 f_{SW} V_{CE(pk)} I_{rr} t_{rr}
\]

(13)

where \( P_{SW} \) is the IGBT Switching loss, \( P_{rr} \) is the diode reverse recovery loss, \( V_{dc} \) is the dc link voltage, \( I_{SW(pk)} \) is the peak current switched by the IGBT, \( I_{SW(on)} \) and \( I_{SW(off)} \) are the IGBT turn-on and turn-off time durations, respectively, \( I_{rr} \) and \( t_{rr} \) are the diode peak reverse recovery current and reverse recovery time, respectively, \( V_{CE(pk)} \) is the peak voltage across the diode at recovery and the switching frequency is \( f_{SW} \). According to the same type of switches and equal switching frequency in both methods, parameters for comparing switching losses are \( V_{dc} \) and \( V_{CE(pk)} \). Reduction percentage of the switching loss is as follows:

\[
R_p \% = \frac{V_{dc(SHM-PWM)} - V_{dc(SHM-PWAM)}}{V_{dc(SHM-PWM)}} \times 100
\]

(14)

Fig. 10. shows the reduction percentage of loss in case 1 versus \( M_a \). \( V_{dc(SHM-PWM)} \) is the dc supply voltage value in case 1 obtained from Fig. 5.C. \( V_{dc(SHM-PWAM)} \) is the dc voltage value used in case 2 which is constant and equal to \( V_{dc} \) in the whole range of \( M_a \). As can be seen from Fig. 10, the switching loss is reduced significantly especially at lower values of \( M_a \).

Fig. 11. shows the flying capacitor voltages in case 1.
Figure 10: Reduction percentage of switching loss in the case 1 versus $M_a$.

Figure 11: Flying capacitor voltages for $M_a = 0.8$ a) capacitor voltage values b) $V_{C1}$ c) $V_{C2}$ and d) $V_{C3}$. 
The corresponding reference values for a typical value of $M_a = 0.8$ are 99, 66 and 33 volts for $V_{C1}$, $V_{C2}$ and $V_{C3}$, respectively. As the SHM-PWAM control strategy is inherently a low-frequency technique, the closed loop method explained in section II is an appropriate choice for balancing the capacitors voltages and has been used in this paper. The maximum acceptable voltage ripple for flying capacitors is considered 5%. It is evident from Fig. 11 that using the voltage closed-loop control closely holds the flying capacitor voltages at their corresponding reference values and the three capacitor voltage ripples are also within the acceptable limits.

To demonstrate the effectiveness of the control method in balancing the flying capacitor voltages according to SHM-PWAM requirements, the value of $M_a$ has been changed at a specific time (from 0.8 to 0.85 at $t = 1.5$ sec). Fig. 12 (a) shows the waveform of the phase leg voltage and Fig. 12 (b) shows the flying capacitor voltages waveform. Despite of the variation of input voltage, control is capable of balancing the output voltage phase A. the flying capacitor voltages reach to their new reference values in less than 0.2 sec.

Figure 12: Step change in the $M_a$ from 0.8 to 0.85 at $t = 1.5$ sec a) the waveform of phase voltage, b) flying capacitor voltages.
Fig. 13 shows the three-phase load current waveform in both cases for $M_a = 0.8$.

The amount of THD is 1.69 and 3.4% in case 1 and 2 respectively. This improvement is due to the improvement of voltage THD in case 1.

**Conclusion**

In this paper the SHM-PWAM control strategy has been applied to a five-level flying capacitor inverter. Realizing SHM-PWAM needs the adjustable dc sources with acceptable dynamic response. The FCMLI has the ability of voltage self-balancing due to its redundancies so it has been chosen for the proposed strategy. Simulation results show the reasonable dynamic of the dc sources values balancing according to the SHM-PWAM requirements. Also a comparison from the THD improvement and loss reduction points of views has proved the SHM-PWAM priority over the conventional one.
References


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